

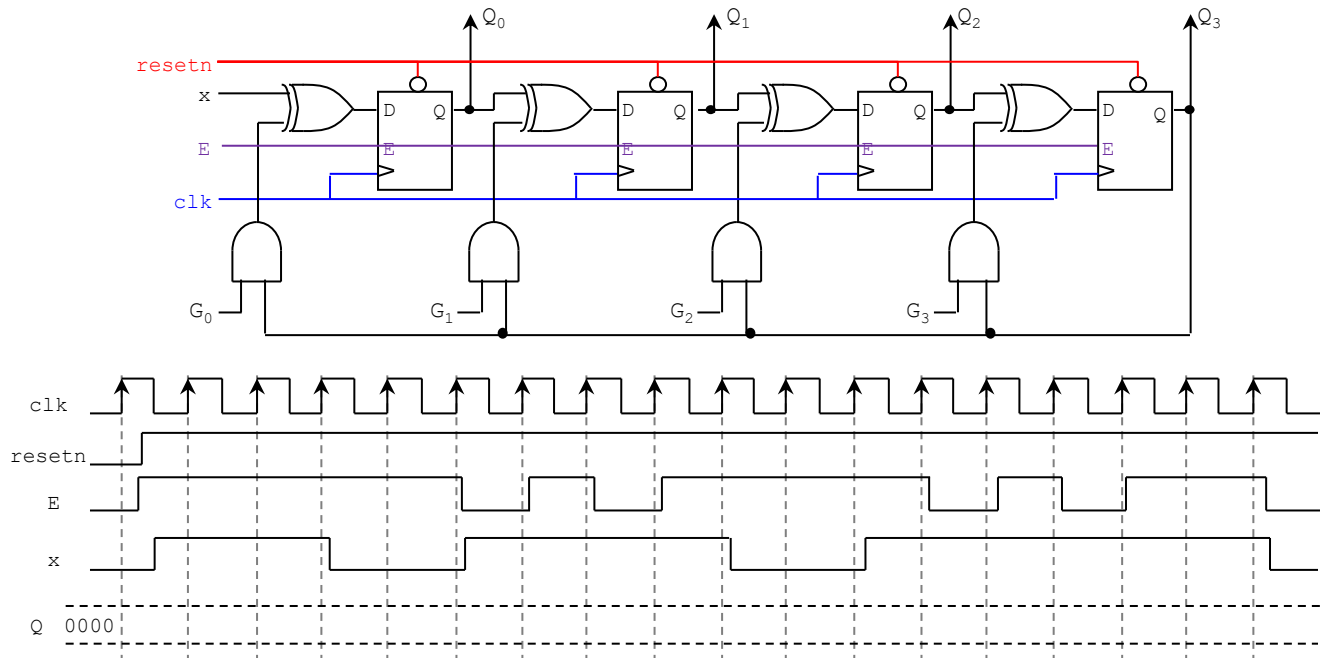
Homework 4

(Due date: March 30th @ 11:59 pm)

Presentation and clarity are very important! Show your procedure!

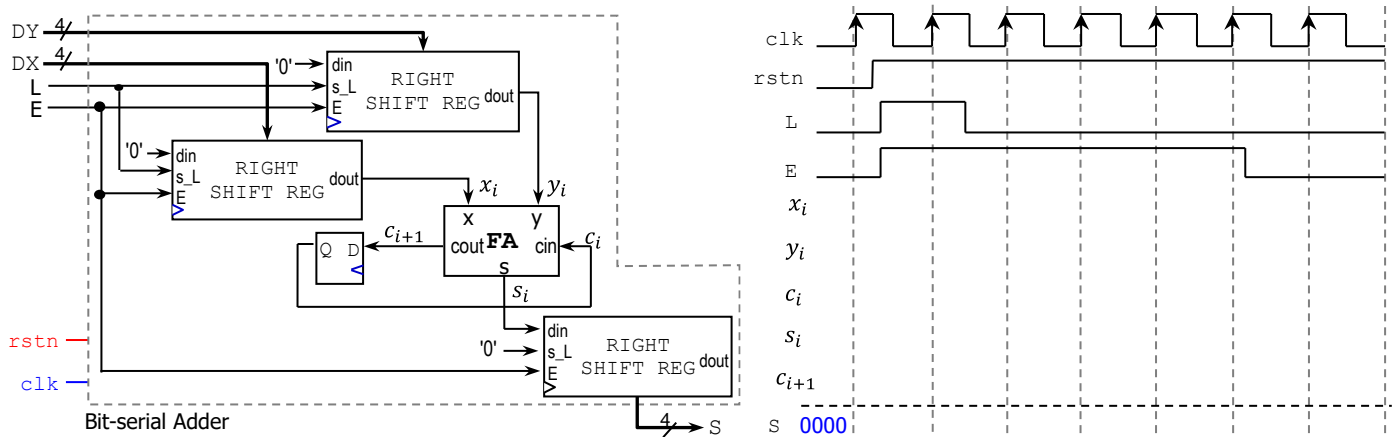
PROBLEM 1 (14 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 1001$, $Q = Q_3Q_2Q_1Q_0$

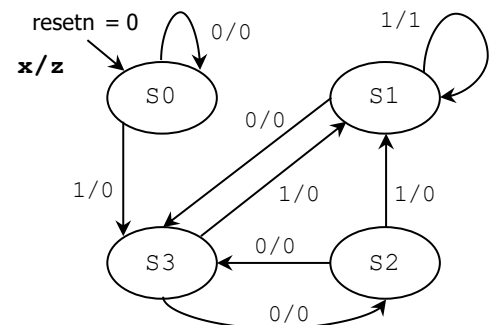


PROBLEM 2 (18 PTS)

- Complete the timing diagram of the following bit-serial adder. $DX=1001$, $DY=1110$. (8 pts)
- ✓ This circuit includes three 4-bit parallel access shift registers, a flip flop, and a full adder.

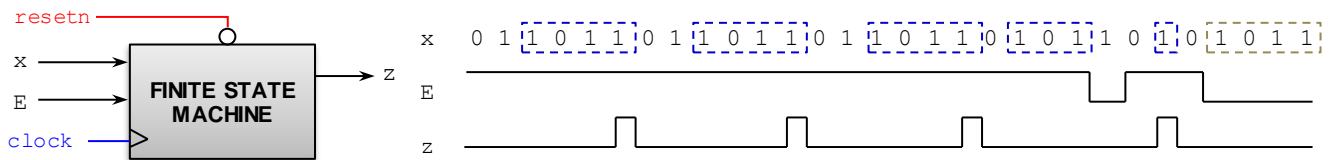


- Given the following State Machine Diagram (10 pts).
- ✓ Is this a Mealy or Moore Machine? Why?
- ✓ Get the excitation equations and the Boolean equation for z. (6 pts)
- Use S0 (Q=00), S1 (Q=01), S2 (Q=10), S4 (Q=11) to encode the states.
- ✓ Sketch the circuit for this Finite State Machine. (3 pts)



PROBLEM 3 (21 PTS)

- Sequence detector: The machine generates $z = 1$ when it detects the sequence 1011. Once the sequence is detected, the circuit looks for a new sequence.
- The signal E is an input enable: It validates the input x , i.e., if $E = 1$, x is valid, otherwise x is not valid.



- Draw the State Diagram (any representation), State Table, and the Excitation Table of this circuit. (14 pts)
- Provide the excitation equations and the Boolean equation for z (simplify your circuit: K-maps or Quine-McCluskey) (4 pts)
- Sketch the circuit. Is this a Mealy or a Moore machine? Why? (3 pts)

PROBLEM 4 (15 PTS)

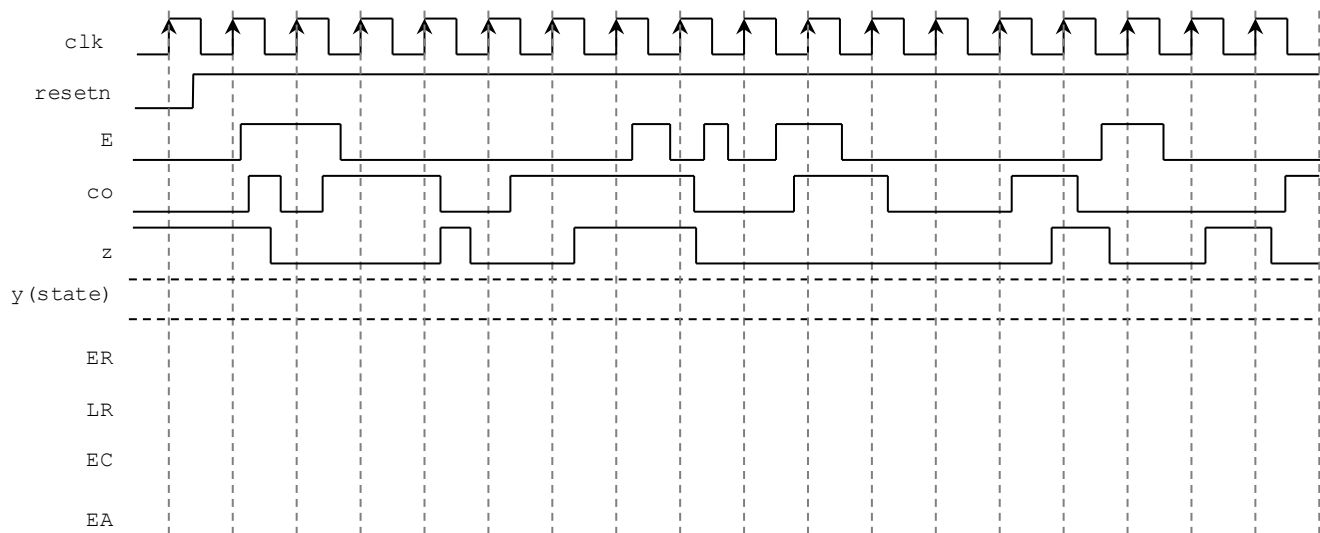
- Draw the State Diagram (in ASM form) of the FSM whose VHDL description is shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

```
library ieee;
use ieee.std_logic_1164.all;

entity myfsm is
    port ( clk, resetn: in std_logic;
          z, E, co: in std_logic;
          ER, LR, EC, EA: out std_logic);
end myfsm;
```

```
architecture behavior of myfsm is
    type state is (S1, S2, S3);
    signal y: state;
begin
    Transitions: process (resetn, clk, z, E, co)
    begin
        if resetn = '0' then y <= S1;
        elsif (clk'event and clk = '1') then
            case y is
                when S1 =>
                    if E = '1' then y <= S2; else y <= S1; end if;
                when S2 =>
                    if z = '1' then y <= S3; else y <= S2; end if;
                when S3 =>
                    if E = '1' then y <= S3; else y <= S1; end if;
            end case;
        end if;
    end process;

    Outputs: process (y, z, E, co)
    begin
        ER <= '0'; LR <= '0'; EC <= '0'; EA <= '0';
        case y is
            when S1 => ER <= '1'; EC <= '1';
                if E = '1' then EA <= '1'; end if;
            when S2 => ER <= '1'; EA <= '1';
                if co = '1' then LR <= '1'; end if;
            when S3 =>
                if z = '0' then EC <= '1'; end if;
        end case;
    end process;
end behavior;
```



PROBLEM 5 (17 PTS)

- Sequential unsigned multiplier: $P = DA \times DB$. Behavior (on the clock tick) of the generic components:

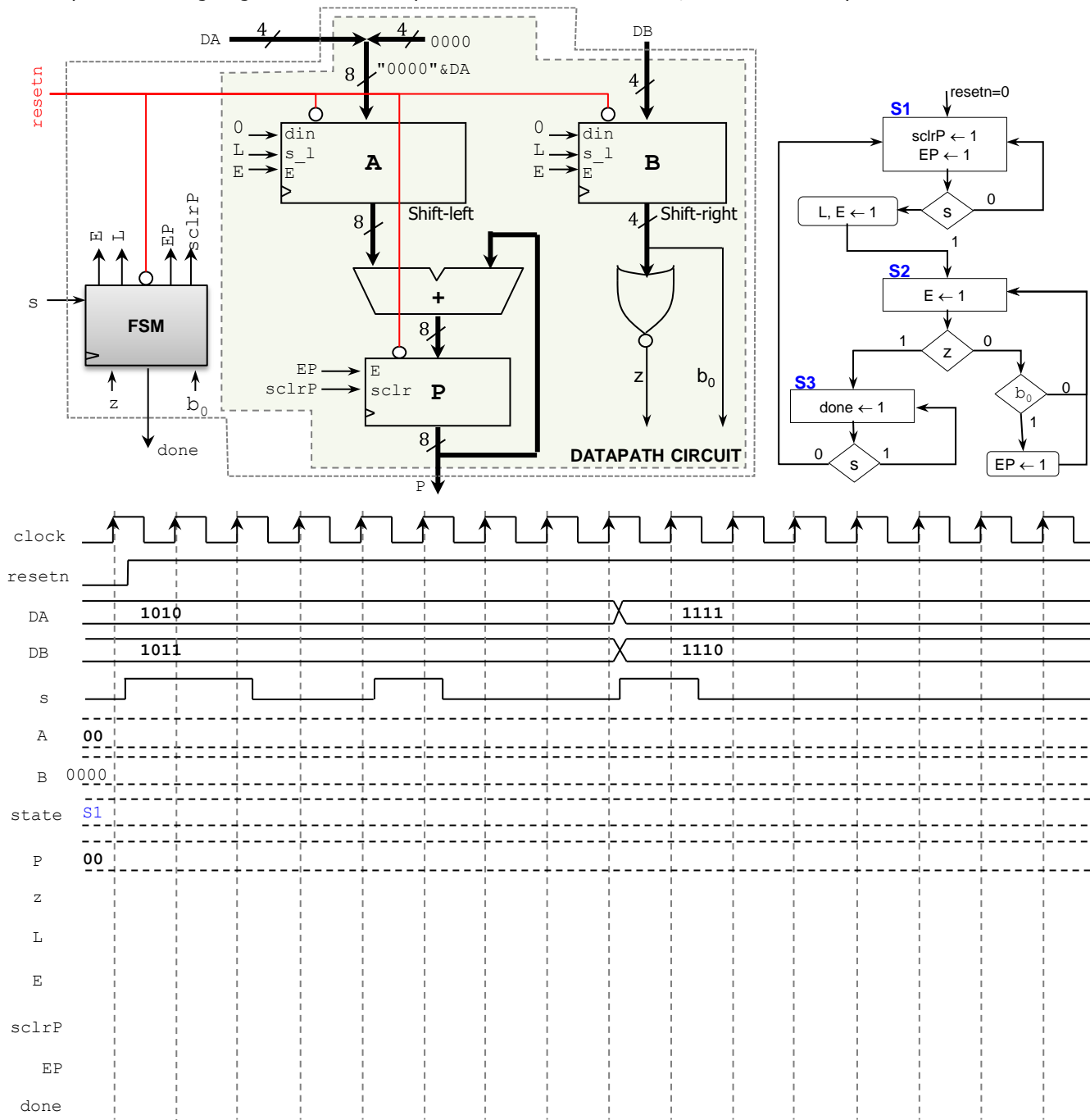
2n-bit register (P): If $E=0$, the output is kept

```
if E = 1 then
  if sclr = 1 then
    Q ← 0
  else
    Q ← D
  end if;
end if;
```

Parallel access shift register (A: 2n bits, B: n bits): If $E=0$, the output is kept

```
if E = 1 then
  if s_l = '1' then
    Q ← D
  else
    Q ← shift in 'din' (to the left (A) or right (B))
  end if;
end if;
```

- Complete the timing diagram. A and P are specified in hexadecimal format, while B is in binary format.



PROBLEM 6 (15 PTS)

- Attach a printout of your Project Status Report (no more than three pages, single-spaced, 2 columns). This report should contain the current status of the project, including more details about its design and components. You **MUST** use the provided template (Final Project - Report Template.docx). * Only one student needs to submit the report.